

What is claimed is:

1. A method of manufacturing a semiconductor integrated circuit device, comprising: (a) the step of irradiating far ultraviolet or vacuum ultraviolet 5 exposure light from a second major surface side of a mask substrate, said mask substrate having on a first major surface thereof a light shielding pattern which is an integrated circuit pattern on a mask and comprises a photo resist pattern; and (b) the step 10 of reduction-projecting, by a projection optical system, said exposure light which has transmitted through said mask substrate, whereby said integrated circuit pattern is imaged on a photo resist film formed on a first major surface of a semiconductor 15 integrated circuit wafer and thus transferred.

2. The method of manufacturing a semiconductor integrated circuit device according to Claim 1, wherein the wavelength of said exposure light is at least 100 nm less than 250 nm.

20 3. The method of manufacturing a semiconductor integrated circuit device according to Claim 2, wherein said wavelength of said exposure light is at least 100 nm but less than 200 nm.

25 4. The method of manufacturing a semiconductor integrated circuit device according to Claim 3,

wherein, in the peripheral portion of the first major surface of said mask substrate, a light screening metal region is provided.

5 5. The method of manufacturing a semiconductor integrated circuit device according to Claim 4, wherein, on the first major surface of said mask substrate, a pellicle is provided so as to cover said integrated circuit pattern, said pellicle being contact-fixed on said light screening metal region.

10 6. A method of manufacturing a semiconductor integrated circuit device, comprising:

(a) the step of irradiating far ultraviolet or vacuum ultraviolet exposure light from a first major surface or a second major surface side of said mask substrate 15 in the state in which the peripheral region of said mask substrate is held on a mask holding mechanism, said mask substrate having on the first major surface thereof a light shielding pattern which is an integrated circuit pattern on a mask and comprises a 20 photo resist pattern, said resist pattern being not provided on said peripheral region; and

(b) the step of reduction-projecting, by a projection optical system, said exposure light which has transmitted through said mask substrate, whereby said 25 integrated circuit pattern is imaged on a photo resist

film formed on a first major surface of a semiconductor integrated circuit wafer and thus transferred.

7. The method of manufacturing a semiconductor integrated circuit according to Claim 6, wherein the wavelength of said exposure light is at least 100 nm but less than 250 nm.

8. The method of manufacturing a semiconductor integrated circuit according to Claim 7, wherein, 10 wherein the wavelength of said exposure light is at least 100 nm but less than 200 nm.

9. The method of manufacturing a semiconductor integrated circuit device according to Claim 8, wherein, in the peripheral portion of the first major 15 surface of said mask substrate, a light screening metal region is provided.

10. The method of manufacturing a semiconductor integrated circuit device according to Claim 9, wherein, on the first major surface of said mask 20 substrate, a pellicle is provided so as to cover said integrated circuit pattern, said pellicle being contact-fixed on said light screening metal region.

11. A method of manufacturing a semiconductor integrated circuit device, comprising:
25 (a) the step of irradiating far ultraviolet or vacuum

ultraviolet exposure light from a first major surface or second major surface side of a mask substrate, said mask substrate having, in an integrated circuit pattern region of the first major surface thereof, a 5 light shielding pattern which is an integrated circuit pattern on a mask and comprises a photo resist pattern and having a light screening metal region provided in the peripheral region of said first major surface; and (b) the step of reduction-projecting, by a projection 10 optical system, said exposure light which has transmitted through said mask substrate, whereby, on a photo resist film formed on a first major surface of a semiconductor integrated circuit wafer, said integrated circuit pattern is imaged and thus 15 transferred.

12. The method of manufacturing a semiconductor integrated circuit device according to Claim 11, wherein the wavelength of said exposure light is at least 100 nm but less than 250 nm.

20 13. The method of manufacturing a semiconductor integrated circuit device according to Claim 12, wherein the wavelength of said exposure light is at least 100 nm but less than 200 nm.

25 14. The method of manufacturing a semiconductor integrated circuit device according to Claim 13,

wherein, on the first major surface of said mask substrate, a pellicle is provided so as to cover said integrated circuit pattern, said pellicle being contact-fixed on said light screening metal region.

5 15. A method of manufacturing a semiconductor integrated circuit device, comprising:

(a) the step of irradiating far ultraviolet or vacuum ultraviolet exposure light from a first major surface or a second major surface side of a mask substrate,

10 said mask substrate having, in an integrated circuit pattern region of the first major surface thereof, a light shielding pattern which is an integrated circuit pattern on a mask and comprises a photo resist pattern, wherein a pellicle is contact-fixed in that 15 part of the peripheral portion of said integrated circuit pattern region in which said photo resist pattern is not formed; and

(b) the step of reduction-projecting, by a projection optical system, said exposure light which has

20 transmitted through said mask substrate, whereby, on a photo resist film formed on a first major surface of a semiconductor integrated circuit wafer, said integrated circuit pattern is imaged and thus transferred.

25 16. The method of manufacturing a semiconductor

integrated circuit device according to Claim 15,
wherein the wavelength of said exposure light is at
least 100 nm but less than 250 nm.

17. The method of manufacturing a semiconductor
5 integrated circuit device according to Claim 16,
wherein the wavelength of said exposure light is at
least 100 nm but less than 200 nm.

18. The method of manufacturing a semiconductor
integrated circuit device according to Claim 17,
10 wherein, in the peripheral portion of the first major
surface of said mask substrate, a light screening
metal region is provided.

19. The method of manufacturing a semiconductor
integrated circuit device according to Claim 18,
15 wherein, on the first major surface of said mask
substrate, said pellicle is contact-fixed on said
light screening metal region.

20. A method of manufacturing a semiconductor
integrated circuit device, comprising:
20 (a) the step of irradiating far ultraviolet or vacuum
ultraviolet exposure light from a first major surface
side or a second major surface side of a mask
substrate, said mask substrate having, on the first
major surface thereof, a halftone light shielding
25 pattern comprising a photo resist pattern which

constitutes an integrated circuit pattern on a mask;
and

(b) the step of reduction-projecting, by a projection
optical system, said exposure light which has

5 transmitted through said mask substrate, whereby, on a
photo resist film formed on a first major surface of a
semiconductor integrated circuit wafer, said
integrated circuit pattern is imaged and thus
transferred.

10 21. The method of manufacturing a semiconductor
integrated circuit device according to Claim 20,
wherein the wavelength of said exposure light is at
least 100 nm but less than 250 nm.

15 22. The method of manufacturing a semiconductor
integrated circuit device according to Claim 21,
wherein the wavelength of said exposure light is at
least 100 nm but less than 200 nm.

20 23. The method of manufacturing a semiconductor
integrated circuit device according to Claim 22,
wherein, in the peripheral portion of the first major
surface of said mask substrate, a light screening
metal region is provided.

25 24. The method of manufacturing a semiconductor
integrated circuit device according to Claim 23,
wherein, on the first major surface of said mask

substrate, a pellicle is provided so as to cover said integrated circuit pattern, said pellicle being contact-fixed on said light screening region.

25. A method of manufacturing a semiconductor integrated circuit device, comprising:

(a) the step of irradiating far ultraviolet or vacuum ultraviolet exposure light from a first major surface side or a second major surface side of a mask substrate, which has, on the first major surface

thereof, a light shielding pattern which is an integrated circuit pattern on a Levenson type phase shift mask and comprises a photo resist pattern; and

(b) the step of reduction-projecting, by a projection optical system, the exposure light which has

transmitted through said mask substrate, whereby, on a first major surface of a semiconductor integrated circuit wafer, said integrated circuit pattern is imaged and thus transferred.

26. The method of manufacturing a semiconductor integrated circuit device according to Claim 25, wherein the wavelength of said exposure light is at least 100 nm but less than 250 nm.

27. The method of manufacturing a semiconductor integrated circuit device according to Claim 26, wherein, wherein the wavelength of said exposure light

is at least 100 nm but less than 200 nm.

28. The method of manufacturing a semiconductor integrated circuit device according to Claim 27, wherein, in the peripheral portion of said first major 5 surface, a light screening metal region is provided.

29. The method of manufacturing a semiconductor integrated circuit device according to Claim 28, wherein, on the first major surface of said mask substrate, a pellicle is provided so as to cover said 10 integrated circuit pattern, said pellicle being contact-fixed on said light screening metal region.

30. A method of manufacturing a semiconductor integrated circuit device, comprising:

(a) the step of irradiating far ultraviolet or vacuum 15 ultraviolet exposure light from a first major surface or a second major surface side of a mask substrate, said mask substrate having, in an integrated circuit pattern region of said first major surface thereof, a light shielding pattern which is an integrated circuit. 20 pattern on a mask and comprises a photo resist pattern, wherein a pellicle is contact-fixed in the peripheral portion of said integrated circuit pattern of said first major surface so as to cover said integrated circuit pattern; and

25 (b) the step of reduction-projecting, by a projection

optical system, said exposure light which has transmitted through said mask substrate, whereby, on a photo resist film formed on a first major surface of a semiconductor integrated circuit, said integrated 5 circuit pattern is imaged and thus transferred.

31. The method of manufacturing a semiconductor integrated circuit device according to Claim 30, wherein the wavelength of said exposure light is at least 100 nm but less than 250 nm.

10 32. The method of manufacturing a semiconductor integrated circuit device according to Claim 31, wherein the wavelength of said exposure light is at least 100 nm but less than 200 nm.

15 33. The method of manufacturing a semiconductor integrated circuit device according to Claim 32, wherein, in the peripheral portion of the first major surface of said mask substrate, a light screening metal region is provided.

20 34. The method of manufacturing a semiconductor integrated circuit device according to Claim 33, wherein, on the first major surface of said mask substrate, a pellicle is provided so as to cover said integrated circuit pattern, said pellicle being contact-fixed on said light screening metal region.

25 35. A method of manufacturing a semiconductor

integrated circuit device, comprising:

(a) the step of irradiating far ultraviolet or vacuum ultraviolet exposure light from a first major surface or a second major surface side of a mask substrate,

5 said mask substrate having, in an integrated circuit pattern region of said first major surface thereof, a light shielding pattern which is an integrated circuit pattern on a mask and comprises a photo resist pattern, wherein a protective film is formed on said 10 photo resist pattern so as to cover said integrated circuit pattern region of said first major surface; and

(b) the step of reduction-projecting, by a projection optical system, said exposure light which has

15 transmitted through said mask substrate, whereby, on a photo resist film formed on a first major surface of a semiconductor integrated circuit wafer, said integrated circuit pattern is imaged and thus transferred.

20 36. The method of manufacturing a semiconductor integrated circuit device according to Claim 35, wherein the wavelength of said exposure light is at least 100 nm but less than 250 nm.

25 37. The method of manufacturing a semiconductor integrated circuit device according to Claim 36,

wherein the wavelength of said exposure light is at least 100 nm but less than 200 nm.